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DOCUMENT
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PCB · LAYER STACK-UP · CONTROLLED IMPEDANCE · SI · REFERENCE DOCUMENT · PUBLIC

PCB stack-up & impedance

Choosing a PCB layer stack and controlling trace impedance — common stack-ups, microstrip vs stripline, return paths, and what to hand the fab.

REVISION	ISSUED	OWNER	COMPANION
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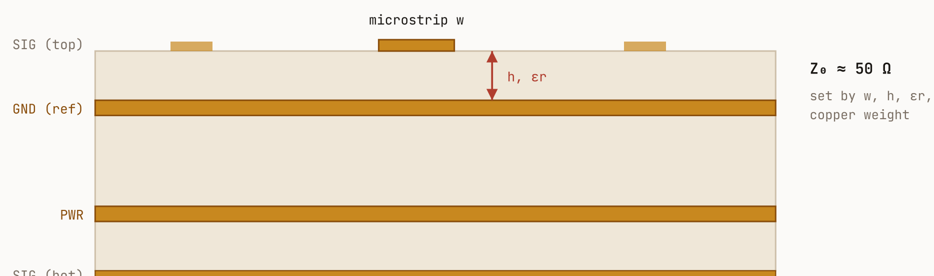
ABSTRACT

The layer stack-up decides a board's signal integrity, power integrity, EMC and cost before a single trace is routed. The two big jobs are giving every signal a continuous reference plane and controlling the impedance of the nets that need it.

Section 1 is what the stack-up is. Section 2 is common stack-ups. Section 3 is controlled impedance (microstrip vs stripline, targets). Section 4 is return paths and power integrity. Section 5 is manufacturing. Section 6 is a checklist.

4-LAYER PCB STACK-UP — MICROSTRIP IMPEDANCE



A 4-LAYER STACK PUTS A GROUND PLANE RIGHT UNDER THE TOP SIGNAL LAYER, SO TRACES HAVE A CLEAN REFERENCE AND CONTROLLED IMPEDANCE. Z_0 IS SET BY TRACE WIDTH, DIELECTRIC HEIGHT, ER AND COPPER WEIGHT.

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1. What the stack-up is
2. Common stack-ups
3. Controlled impedance
4. Return paths and power integrity
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1. What the stack-up is

A PCB is alternating **copper layers** and **dielectric** (FR4 core and prepreg). The arrangement — how many copper layers, which are planes, and the spacing between them — sets impedance, the quality of power delivery, EMC, and board cost. Decide it **first**, with the fab.

Core / prepreg	Cured glass-epoxy (core) and the bonding layers (prepreg) between coppers
Reference plane	A solid GND (or power) plane that a signal's return current flows in
Microstrip	A trace on an outer layer, referenced to one plane below
Stripline	A trace on an inner layer, between two planes
εr	Dielectric constant of the laminate (~4.2–4.5 for FR4) — a key impedance driver

2. Common stack-ups

LAYERS	TYPICAL ARRANGEMENT	USE
2	Sig / Sig	low-speed, low-cost; add a ground pour, but no true plane
4	**Sig / GND / PWR / Sig**	the workhorse — clean references, good SI
6	Sig / GND / Sig / Sig / PWR / Sig	denser routing with planes
8+	more plane pairs	high-speed, HDI, many supplies

Put a **ground plane directly under the top signal layer** (the value of 4-layer over 2-layer). Keep the stack **symmetric** about the centre so the board doesn't warp in reflow.

3. Controlled impedance

High-speed nets must hit a target characteristic impedance, set by the geometry:

- **Microstrip (outer layer, one reference plane) vs stripline (inner, between two planes**
  better shielded, slightly slower).
- **What sets Z_0: wider trace → lower Z; thicker dielectric to the plane → higher Z; higher εr → lower Z; heavier copper → slightly lower Z.**

NET	TARGET IMPEDANCE
Single-ended (general)	50 Ω
USB 2.0 / USB-3 pairs	90 Ω differential
Ethernet / LVDS	100 Ω differential
HDMI / DisplayPort	100 Ω differential
Video (coax-fed)	75 Ω

Don't hand-calculate final widths — give the fab the **impedance targets and which layers**, and let them set trace width/spacing for their actual laminate.

4. Return paths and power integrity

- **Every signal returns in the plane beneath it. Keep a continuous reference plane directly under each fast trace.**
- **Don't route across plane splits**
  the return current can't follow, creating a loop antenna (EMC failure) and reflections. If you must cross, add a **stitching capacitor** between the planes near the crossing.
- **Decouple at the pins: 100 nF per IC power pin, close, plus bulk; tight power-to-ground plane spacing lowers plane impedance.**
- **Stitching vias tie ground planes together and give return vias a nearby path when a signal changes layers.**

5. Manufacturing

- Laminate: standard FR4 (εr ≈ 4.3, choose Tg for lead-free reflow); special low-loss laminates for RF/very-high-speed.
- Copper weight: 0.5 oz (17 µm), 1 oz (35 µm) default, 2 oz for power.
- Min trace/space: ~0.1 mm (4 mil) standard, down to ~0.075 mm advanced; respect the fab's class and your copper weight.
- Drills / aspect ratio: keep hole aspect ratio (board thickness / drill) within the fab's limit; specify finish (HASL for cost, ENIG for fine-pitch/flatness).

6. Checklist

- **Layer count from speed + routing density (4-layer is the sensible default for anything with a fast bus).**
- **Reference planes**
  solid GND under the top signal layer; symmetric stack.
- **Controlled-impedance nets**
  list them, their target Z and layer, and put it on the fab notes.
- **Return paths**
  no splits under fast traces; stitching caps/vias where layers or planes change.
- **Decoupling**
  100 nF per power pin + bulk; tight power/ground spacing.
- **Fab notes**
  laminate, copper weight, impedance table, finish, class. Pairs with the
  Resistor/capacitor
  and
  EMC
  references.