EMC · ESD · GROUNDING · FILTERING · REFERENCE DOCUMENT · PUBLIC

ESD & EMC design checklist

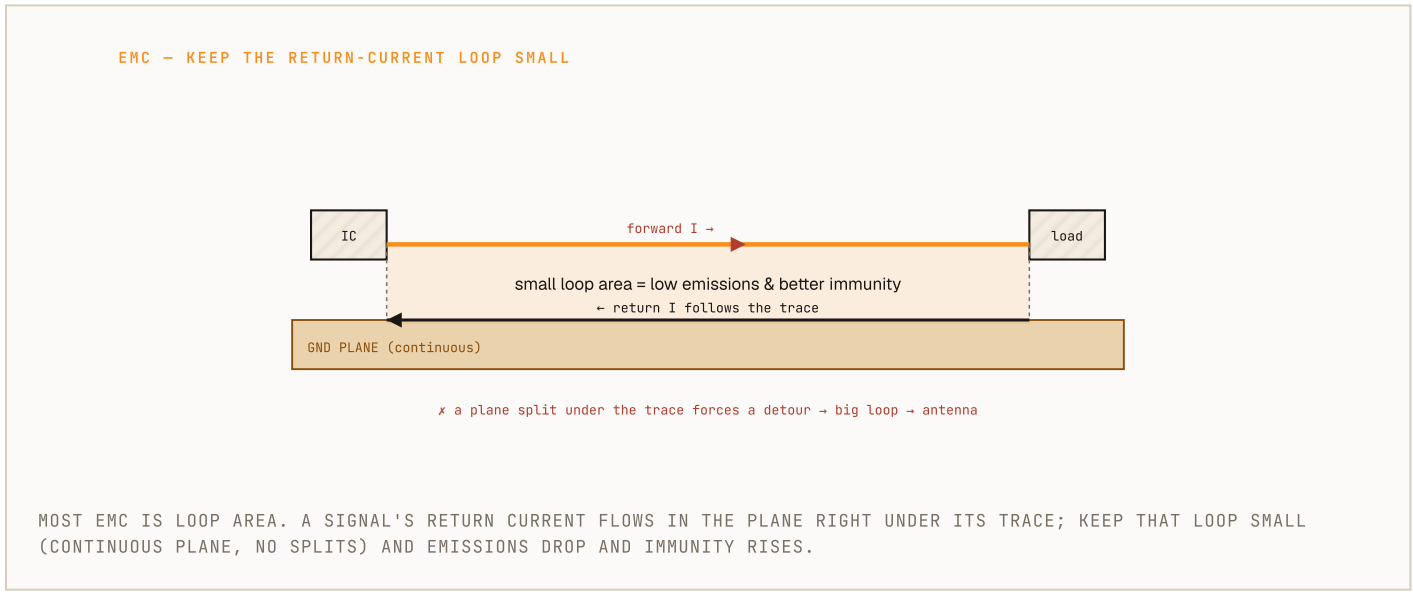
Designing electronics to pass EMC and survive ESD — grounding and return paths, filtering and decoupling, layout, and I/O protection — before the test lab.

REVISION	ISSUED	OWNER	COMPANION
1.0	June 2026	Ideambox engineering	PDF reference

ABSTRACT

EMC and ESD are won at design time, not at the test lab. Emissions and immunity both come down to controlling current loops, grounding and filtering; ESD comes down to giving the discharge a safe path and clamping exposed I/O. This is the design checklist.

Section 1 frames the threats. Section 2 is grounding and return paths. Section 3 is filtering and decoupling. Section 4 is layout. Section 5 is ESD protection. Section 6 is cables, shielding and a checklist.



MOST EMC IS LOOP AREA. A SIGNAL'S RETURN CURRENT FLOWS IN THE PLANE RIGHT UNDER ITS TRACE; KEEP THAT LOOP SMALL (CONTINUOUS PLANE, NO SPLITS) AND EMISSIONS DROP AND IMMUNITY RISES.

CONTENTS

1. The threats

EMC has two sides — **emissions** (don't pollute) and **immunity** (don't be disturbed) — plus discrete events like **ESD**:

PHENOMENON	STANDARD	FIRST-LINE DEFENSE
Radiated emissions	CISPR 32	small loops, slow edges, shielding, filtering
Conducted emissions	CISPR 32	input/power-line filter, decoupling
ESD	IEC 61000-4-2	TVS on I/O, ground rings, creepage, discharge path
Electrical fast transient (burst)	61000-4-4	power-entry filtering, decoupling
Surge	61000-4-5	MOV / TVS clamping, series impedance
Radiated immunity	61000-4-3	shielding, I/O filtering, robust firmware

`Loop area`	Area enclosed by a signal and its return — the dominant emissions driver
`Decoupling`	Local capacitance that supplies an IC's fast current so it isn't drawn through long loops
`Common-mode`	Noise on all conductors together (vs differential) — the usual EMC culprit on cables
`TVS`	Transient-voltage-suppression diode that clamps ESD/surge on an I/O line

2. Grounding and return paths

- **One solid ground plane under everything; let return current flow directly beneath each trace (smallest loop).**
- **Don't split the plane under signals**
  a slot forces the return to detour, making a big loop (an antenna) and a noise voltage across the gap.
- **Partition noisy (switchers, motors, clocks) from quiet (analog, RF) areas, but keep a continuous reference; use a single connection point between domains only when truly needed.**
- **Chassis vs signal ground: bond deliberately (often at the connector/entry) so ESD and shield currents go to chassis, not through the board.**

3. Filtering and decoupling

- **Decouple every IC power pin with a local HF capacitor (100 nF) plus bulk; this keeps fast current loops tiny (see Resistor/capacitor reference for dielectrics).**
- **Filter at the connector / board edge**
  ferrites and common-mode chokes on cables, pi/LC filters on power and I/O — stop noise before it reaches a cable that radiates.
- **Series resistors / source termination slow edges and damp ringing on fast lines (lower harmonics = lower emissions).**
- **Power-entry filter for conducted emissions and EFT/surge robustness.**

4. Layout for EMC

- **Minimize loop area everywhere**
  adjacent signal/return, traces over continuous planes.
- **Slow the edges you don't need fast; contain clocks (short, guarded, away from edges/connectors).**
- **Keep crystals/oscillators local, guarded, with a ground pour and away from board edges and I/O.**
- **Route I/O and high-speed over their reference plane, never over a plane gap.**
- **Guard / shield sensitive nets; keep noisy nets away from cables and the board edge.**

5. ESD protection

- **Clamp every exposed I/O (connectors, buttons, USB, antennas) with a TVS rated for the line; place it at the entry, with a short, low-inductance path to chassis/ground.**
- **Series impedance (small R or ferrite) after the clamp limits residual energy into the IC.**
- **Ground/guard rings around exposed conductive parts; respect creepage/clearance so the arc goes where you want.**
- **Give ESD a path to chassis that bypasses sensitive circuitry**
  buttons, shields and seams should discharge to chassis ground.

6. Cables, shielding and checklist

- **Cables are the antennas**
  filter and common-mode-choke I/O at the connector; **360° shield termination** (not a pigtail) to chassis.
- **Enclosure: seams and apertures act like slot antennas above their resonant frequency**
  keep openings small, use gaskets/fingerstock on shielded enclosures, and bond panels.
- **Checklist: solid continuous ground plane · small loops, no splits under signals · decouple every power pin · filter + CM-choke at every cable entry · slow unnecessary edges · TVS + series R on every exposed I/O · 360° shield bonds · partition noisy/quiet · plan the ESD path to chassis. Pre-scan early**
  fixing EMC after layout is expensive (see
  EMC pre-compliance
  , IDB-EMC-016).