

EMC design and pre-compliance

Reference for designing for electromagnetic compatibility from the start — applicable standards, in-design rules for grounding, shielding, filtering, and the pre-compliance workflow that catches failures before formal lab time.

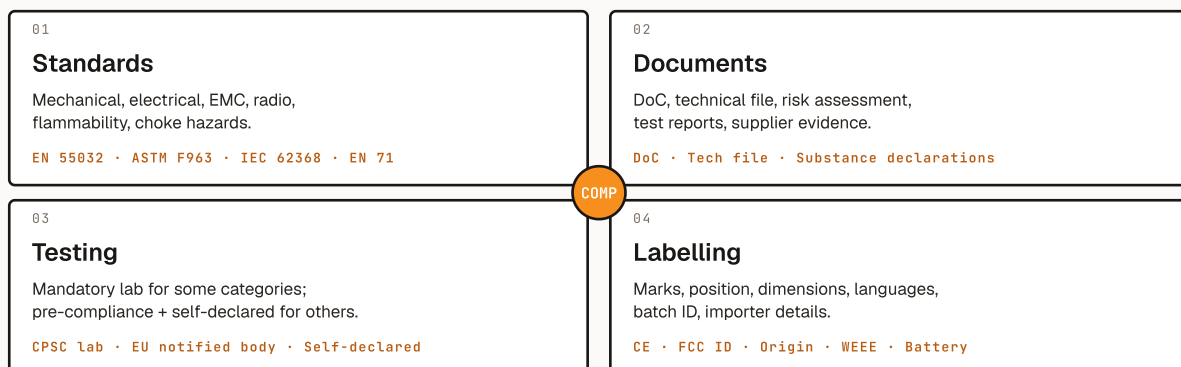
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ABSTRACT

EMC (Electromagnetic Compatibility) failures account for ~40 % of first-pass lab failures in consumer electronics. The fix is design discipline at schematic + PCB layout, plus a pre-compliance scan workflow that catches issues at \$300–800 per scan instead of \$3 000–8 000 per failed lab booking.

Section 1 covers applicable standards (EN 55032, EN 55035, FCC Part 15, etc.). Section 2 covers grounding and ground topology. Section 3 covers shielding strategies. Section 4 covers filtering (decoupling, ferrite beads, common-mode chokes). Section 5 covers ESD protection. Section 6 covers the pre-compliance workflow. Section 7 catalogues common failures and fixes.

THE FOUR ELEMENTS OF COMPLIANCE



EMC IS ONE OF THE FOUR PILLARS OF COMPLIANCE. THE OTHER THREE (DOCUMENTS, TESTING, LABELLING) ARE ADDRESSED BY IDB-PSC-002.

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1. EMC standards

Different standards apply to emission (your device leaking) and immunity (external interference reaching your device). Both must pass for CE / FCC compliance.

1.1 Emission standards (radiated + conducted)

STANDARD	REGION	SCOPE	FREQUENCY RANGE
EN 55032 / CISPR 32	EU + global	Multimedia equipment	9 kHz – 6 GHz
EN 55014-1	EU	Household appliances	9 kHz – 30 MHz conducted; 30 MHz – 300 MHz radiated
FCC Part 15 Class A	US	Industrial, commercial	9 kHz – 40 GHz
FCC Part 15 Class B	US	Residential	More stringent than Class A
EN 55015	EU	Lighting	9 kHz – 30 MHz
CISPR 11 / EN 55011	Global	Industrial, scientific, medical	9 kHz – 18 GHz

1.2 Immunity standards

STANDARD	TEST	LEVEL
EN 55024	Multimedia equipment immunity	Defined by EN 55035
EN 55035	Multimedia equipment immunity	2017 revision; current EU
IEC 61000-4-2	ESD	±8 kV contact / ±15 kV air (level 4)
IEC 61000-4-3	Radiated immunity	3 V/m typical; 10 V/m for industrial
IEC 61000-4-4	Electrical fast transient (EFT)	±1–4 kV per port
IEC 61000-4-5	Surge	±0.5–4 kV
IEC 61000-4-6	Conducted immunity	3 V (rms) per port
IEC 61000-4-8	Power frequency magnetic field	30 A/m
IEC 61000-4-11	Voltage dips and short interruptions	0–95 % depth

1.3 Frequency vs. wavelength reference

FREQUENCY	WAVELENGTH (λ)	NOTES
30 MHz	10 m	Beginning of radiated emission band (CISPR)
100 MHz	3 m	Common clock harmonics
1 GHz	30 cm	Wi-Fi 2.4 GHz; antenna analyses begin
6 GHz	5 cm	Upper EN 55032 / FCC Part 15 limit
24 GHz	1.2 cm	mmWave radio; 5G n258 band

Slot apertures $> \lambda/20$ act as antennas. At 1 GHz, 1.5 cm slot leaks; at 6 GHz, 2.5 mm slot leaks.

2. Grounding + ground topology

Ground topology determines EMC performance. Most EMC failures trace back to ground design.

2.1 Three grounding philosophies

TOPOLOGY	BEST FOR	COMMON FAILURE
Single ground plane	Digital + most analog	Splitting under high-speed traces
Star ground	Mixed-signal (audio, ADC)	Multiple star points creating loops
Multi-point ground	Frequencies > 1 MHz	Insufficient short paths to common

2.2 Single ground plane rules

- **Solid copper pour on a dedicated layer. No traces, no splits.**
- **Connect every component ground to the plane through one via per ground pin (more for high-current ICs).**
- **Adjacent power planes create a low-impedance plane pair that handles return currents naturally.**
- **Cuts and splits create EMC problems**
Forces return current to take long paths, increases loop area, radiates strongly.

2.3 Common ground topology mistakes

- **Splitting ground for "thermal isolation"**
Creates antenna-like structures. Use thermal vias or copper polyimide instead.
- **Cutting ground under fast-edge signals**
Return current diverts to nearest path; loop area grows.
- **No chassis-to-PCB ground connection**
Static charge has no return path; ESD damage likely.
- **Multiple ground vias far from each other**
Creates ground bounce. Add adjacent vias for low impedance.
- **Star ground at multiple frequencies**
Star is only stable at low frequencies; at RF, requires careful loop design.

2.4 Return current behaviour

Every signal trace has a return current that follows the path of least impedance. At high frequencies, this means **directly under the signal trace** (lowest inductance), not the lowest-resistance path.

A "ground plane" cut under a high-speed trace forces the return current to go around the cut, increasing loop area dramatically and radiating EMI.

3. Shielding

Shielding reduces both emission (containment) and immunity (rejection). Choose based on target frequency and budget.

3.1 Shielding strategies

STRATEGY	COST	EFFECTIVENESS
Local shielding cans (over RF / DC-DC)	\$0.20–2.00 each	20–60 dB at GHz
Full enclosure shield (metal box, foil bag)	Higher	40–80 dB
EMI gaskets at openings	\$0.50–5.00 each	Maintains seal at apertures
Conductive paint (on plastic enclosure)	Inexpensive coating	10–30 dB
Metallised plastic enclosure (PVD/sputter)	Adds 10–20 % to part cost	30–50 dB
Plated/embedded ferrite cable shield	Per cable	10–30 dB on cables

3.2 Shielding rules

- **Enclose at the source**

Shield the noise generator (DC-DC, oscillator, microprocessor), not the rest of the board.

- **Slot apertures matter**

Above $\lambda/20$ they radiate. Maximum slot size at 1 GHz: ~15 mm. At 6 GHz: ~2.5 mm.

- **Cable shields**

Connect to chassis at both ends for high-frequency shielding (the lower-frequency loop concern doesn't apply at GHz).

- **Vent holes**

Many small holes radiate less than one large hole. Honeycomb vents reduce leakage further.

3.3 Common-mode chokes for cables

USB, audio, and other cables can act as antennas. Common-mode chokes on cable inputs reduce conducted emissions:

- **USB CMC**

0.1 μ H (rated at 100 MHz) for USB 2.0/3.0

- **Power input CMC**

1–10 mH for AC power

- **Audio CMC**

Per channel for cleaner audio

4. Filtering + decoupling

Internal filtering at the PCB level catches conducted emissions before they reach cables.

4.1 Decoupling cap placement

- One ceramic 100 nF per VCC pin of every IC. Within 5 mm of the pin.
- One bulk cap (1–10 μ F) per power-rail bank.
- Multiple ceramics in parallel (10 nF + 100 nF + 1 μ F) at high-current IC pins.
- Place caps on the bottom layer adjacent to the IC, with through-hole connection to power plane.

See IDB-PCB-014 for detail on decoupling strategy.

4.2 Ferrite beads

Ferrite beads add impedance at RF frequencies while passing DC and low-frequency current.

TYPE	IMPEDANCE @ 100 MHz	USE
Small (0402, 0603)	60–600 Ω	Signal lines, low-current
Medium (0805, 1206)	60–1 000 Ω	Power lines (<1 A)
Large (1812, 2220)	600–3 000 Ω	Power input filters
High-current (chip 1812 or larger)	30–600 Ω	DC-DC regulator outputs

Ferrite beads on power lines are usually placed at the regulator input/output, not at every IC.

4.3 Π -filters

Combine ferrite bead + capacitor for stronger filtering.

“ Ferrite IN ——— [FB] ——— OUT | | C₁ (100 nF) C₂ (100 nF) | | GND GND ”

Attenuates conducted emissions by 20–40 dB at 100 MHz.

5. ESD protection

ESD = Electrostatic Discharge. The transient is fast (<1 ns rise time) but high amplitude (8–15 kV).

5.1 ESD test levels (IEC 61000-4-2)

LEVEL	CONTACT DISCHARGE	AIR DISCHARGE
1	±2 kV	±2 kV
2	±4 kV	±4 kV
3	±6 kV	±8 kV
4	±8 kV	±15 kV

Level 4 is the typical requirement for consumer products with accessible signals.

5.2 ESD protection devices

DEVICE	USE	SELECTION
TVS array	USB-C, audio jack, exposed connector	Per data rate (12 V or 24 V clamp)
Bidirectional TVS	AC signal (audio)	Symmetric clamp
ESD diode (TVS chip-scale)	Single signal pin	0402 / 0201 package
RC filter	Slower interfaces (I2C, UART)	Series R + shunt C
Suppressor (transient)	High-power lines	Beyond TVS capability

5.3 ESD protection placement

- **Place TVS at the connector, not at the IC. Clamps the surge before it propagates.**
- **TVS to ground via short trace**
Minimise trace length to reduce inductance.
- **Multiple TVS for high pin count**
Don't bottleneck on one device.

5.4 TVS selection criteria

- **Standoff voltage (V_R)**
Must be higher than the maximum normal signal voltage.
- **Breakdown voltage (V_{BR})**
Typically 5–25 % above V_R.
- **Clamping voltage (V_C) at 8/20 μs pulse**
The voltage at which the TVS clamps. Lower V_C = better protection.
- **Capacitance (C)**
Lower C is better for high-speed signals (USB 3.0+ requires <0.5 pF).

5.5 Common ESD failure modes

- **No TVS**
IC pin damaged, intermittent or hard failure.
- **TVS placed at IC, not at connector**
Surge propagates between connector and TVS, can damage trace.

- **Insufficient TVS capacity**

Common in USB-C where multiple pins need protection.

- **Single-pin TVS used on differential pair**

Asymmetric clamping, can corrupt data.

6. Pre-compliance workflow

Catching EMC issues in-house before formal lab testing saves \$3 000–8 000 per failure cycle.

6.1 Pre-compliance test setup

COMPONENT	COST	USE
Spectrum analyser (9 kHz – 6 GHz)	\$5 000–25 000	Radiated + conducted scans
Near-field probe set (H + E field)	\$300–1 000	Locating noise source
Current probe (clamp-on)	\$500–2 000	Cable conducted current
RF turntable or test chamber	\$5 000–50 000	Reproducible measurements
ESD gun (8 kV contact / 15 kV air)	\$2 000–5 000	IEC 61000-4-2
Surge generator	\$5 000–15 000	IEC 61000-4-5
Spectrum analyser software	\$1 000–5 000	Compliance limit overlay

A budget pre-compliance setup (~\$8 000–15 000) catches 70 % of issues that would otherwise fail formal lab testing.

6.2 Pre-scan workflow

1. **Power up the DUT (Device Under Test)** in worst-case mode (max Wi-Fi traffic, max CPU load, charging, etc.). 2. **Measure conducted emissions** on power line — Common above 150 kHz to 30 MHz. 3. **Measure radiated emissions** in a quiet room (ideally semi-anechoic) — 30 MHz to 6 GHz. 4. **Compare to standards limits** (CISPR 22 / 32 / FCC Part 15 Class B). 5. **Identify worst-case bands and frequencies.** 6. **Apply candidate fixes** (filtering, shielding, layout change) and re-measure. 7. **Pass/fail decision** before booking the lab.

6.3 When to schedule pre-compliance

- **First proof-of-concept**
Quick scan to see worst-case noise.
- **Pre-production sample**
Definitive pre-scan; identify all issues.
- **Re-test before formal lab**
Confirm all fixes hold.

7. Common EMC failures + fixes

The top 80 % of EMC failures fall into 5 categories.

7.1 Conducted emissions on USB power

SYMPTOM	CAUSE	FIX	COST
Failure 150 kHz–10 MHz on USB power	Switching regulator noise reaching USB	Add CMC + bulk caps at USB input	\$0.05–0.20/unit
Failure at switching frequency harmonics	Insufficient input filtering	Larger input cap or ferrite bead	\$0.10–0.30/unit
Failure during heavy load	Inductor saturation	Larger inductor or different core	Inductor swap

7.2 Radiated emissions 30 MHz – 1 GHz

SYMPTOM	CAUSE	FIX	COST
Cable acting as antenna	Common-mode current on cable	Ferrite bead or shielded cable	\$0.10–1.00/unit
Crystal harmonic radiation	Direct radiation from oscillator	Shield over crystal, shorter traces	\$0.50–2.00/unit
Logic gate switching noise	Open trace runs on outer layer	Move signal to inner layer	Layout rework

7.3 Radiated emissions > 1 GHz

SYMPTOM	CAUSE	FIX
PCB clock harmonics	Direct radiation from clock	Spread-spectrum modulation in MCU firmware
RF subharmonics	Mixed-signal coupling	Better ground plane isolation
Mobile phone interference	EMC immunity issue	Move sensitive circuits away from sources

7.4 ESD failure on USB-C

SYMPTOM	CAUSE	FIX	COST
Device hangs or reboots on ESD	No TVS or TVS too late	Add TVS array at connector	\$0.30–0.80/unit
Smoking IC after ESD	TVS rated too low or no clamping	Higher current TVS, ferrite series resistor	\$0.40–1.20/unit

7.5 Burst immunity on sensor input

SYMPTOM	CAUSE	FIX
Long unshielded sensor cable picks up burst	Common-mode coupling	Differential drive + filter at sensor end
Multi-foot I2C bus susceptible	Pull-ups too weak	Add series resistor + lower pull-up

FINAL NOTE. EMC is engineering's least-glamorous discipline. Most consumer electronics product launches that "ship late" had their final blocker in EMC lab. The fix is invariably "designed-in" — schematic and PCB-layout decisions made months earlier. The 1-2 weeks an engineer invests in EMC design discipline at PCB layout time pays back 10× in saved lab fees and shipped product.